A Class-B Push-Pull Power Amplifier Based on an Extended Resonance Technique

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***Abstract*—A class B push-pull power amplifier based on an extended resonance power combining technique is presented. In this design, advantages of push-pull power amplifier, such as doubling power capability and reduced common lead effects, have been achieved with a simple and compact circuit topology. The measured power combining efficiency (PCE) is 93% with 1-dB bandwidth of 12.6% at 1.75 GHz. The measured output power at 1-dB compression is 30 dBm with power added efficiency (PAE) of 59%.**

***Index Terms*—Class B, extended resonance, power amplifier, push-pull.**

I. Introduction

In THE wireless-communication systems, push-pull power amplifier designs were originally proposed because of their high efficiency and linearity [1]. However, the 180° hybrids or baluns required in the conventional push-pull architectures limit their applications at RF/microwave frequencies. Not only the required quarter wavelength transmission lines and pre-matching circuits for each active device consume large layout area, but also insertion loss of baluns or 180° hybrids degrade the overall efficiency. Several new push-pull architectures have been proposed, including a class C push-pull PA for X-band with $TE_{01\delta}$ mode dielectric resonators [2], a class AB push-pull amplifier using periodic structures for harmonic tuning [3], and broad-band push-pull amplifier based on Marchand balun [4]. These designs improve the efficiency and the linearity of push-pull power amplifiers at RF/microwave frequencies. However, these techniques still require pre-matching circuits between the 50-Ω environments and the complex impedances at transistors.

As proposed in our previous papers [5]–[7], an extended resonance technique can be employed to achieve high power combining efficiency using simple and compact circuit topology. In this technique, equal power combining/dividing is achieved by designing circuits that resonate input and output admittances of multiple active devices.

In this paper, the extended resonance technique has been employed to design a class B push-pull PA by introducing a T-shaped network between active devices (Fig. 1). This topology allows flexibility in controlling the phase delays between two active devices and optimizing the entire circuit's performance [5]. In addition to the advantages mentioned, the push-pull architecture will reduce the common lead effects at the transistor sources, especially for chip level applications [1].

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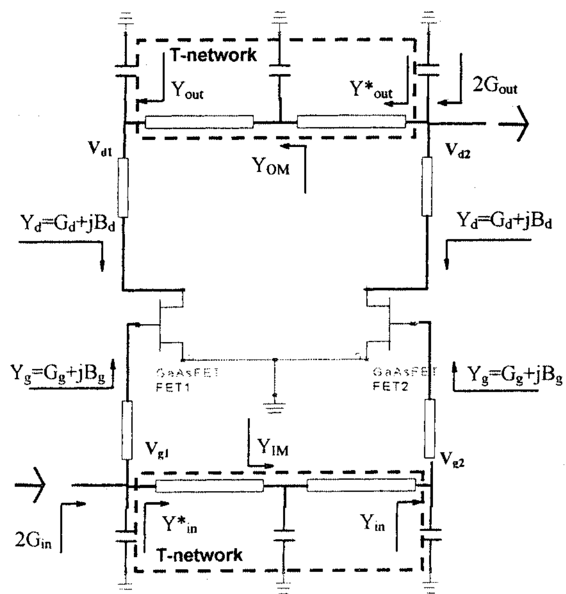

Fig. 1. Class B push-pull power amplifier based on extended resonance technique.

II. Design Process

As discussed in [5]–[7], both transmission-line and lumped-element topologies can be used for extended resonance power amplifier design. For the design in this paper, the transmission line circuit approach has been used. Based on the extended resonance technique, the admittance at one transistor's gate/drain is transformed using a series lumped element or transmission line to its conjugate value at the adjacent device's gate/drain. Thereby, the combined gate and drain line admittances are pure real values, which can easily be matched to 50-Ohms. This type of circuit results in an equal power dividing/combining network [6]. The input dividing and output combining circuits are designed separately with a phase shift of 180° between two active devices for push-pull operation. The 180° phase delay can be obtained with transmission lines that are much shorter than half wavelength. The circuit diagram of an extended resonance push-pull power amplifier is shown in Fig. 1. The voltage ratios of V_{g1}/V_{g2} and V_{d1}/V_{d2} (Fig. 1) can be calculated using the following relations [7]:

$$\frac{V_1}{V_2} = \frac{1}{A} \times \frac{1}{B} \tag{1}$$

$$A = (\cos\beta l - B\sin\beta l + jG\sin\beta l) \tag{2}$$

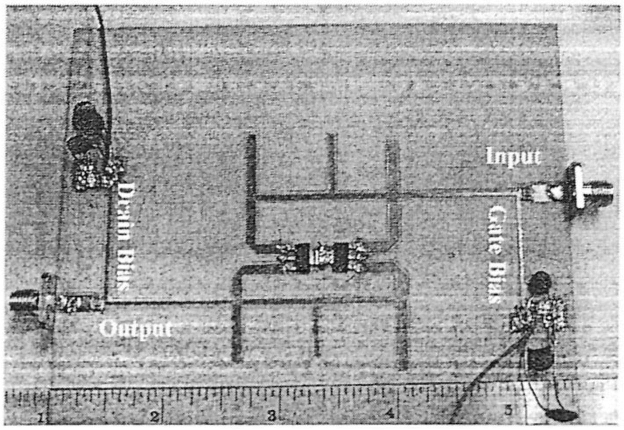

Fig. 2. Layout for the class B push-pull amplifier at 1.75 GHz.

$$B = (\cos\beta l - B_{\rm M}\sin\beta l + jG_{\rm M}\sin\beta l) \qquad (3)$$

where, for the input network, $Y_{\rm in} = G + jB$ and $Y_{\rm IM} = G_{\rm M} + jB_{\rm M}$; and for the output network, $Y_{\rm out} = G + jB$ and $Y_{\rm OM} = G_{\rm M} + jB_{\rm M}$. Based on these formulas, the shunt capacitor susceptance of $-2jB_{\rm M}$ results in an equal power division/combination (i.e., $|V_1/V_2| = 1$) and a phase delay of:

$$\frac{\angle V_1}{\angle V_2} = -2\arctan\left(\frac{G\tan\beta l}{1 - B\tan\beta l}\right). \qquad (4)$$

According to (4), $\beta l = \arctan(1/B)$ results in a 180° phase delay between two transistors. The input and output admittances (Y_g and Y_d) at the gate and drain of the transistors are determined based on load-pull simulations of the GaAs MESFET's nonlinear model to maximize the power added efficiency (PAE) of this class-B power amplifier. By adjusting admittances, $Y_{\rm in}$ and $Y_{\rm out}$, this design can be optimized for bandwidth.

III. Experiment Results

Based on the theory described in the previous section, a class B push-pull power amplifier was designed and fabricated (Fig. 2). In this design, two packaged GaAs MESFET's (Siemens model CLY5) were used. The circuit was fabricated on a 60-mil-thick Duroid substrate with $\varepsilon_r = 2.94$ and $\tan\delta = 0.0012$. Simulations of circuit were performed on Serenade 8.5 (Ansoft Inc.). Based on load-pull simulations using a the nonlinear Materka model for the device, the optimized output power ($P_{\rm out}$) of 27.6 dBm at 1dB gain compression was predicted from the single class B amplifier with a PAE around 65% at 1.75 GHz. The corresponding load and source admittances were $Y_{\rm load} = 0.025 - j0.041$ S and $Y_{\rm source} = 0.036 - j0.052$ S. The shunt capacitors in Fig. 1. have been replaced by open circuited stubs to simplify the fabrication.

The simulated gate voltage and drain voltage waveforms for each device in the extended resonance push-pull amplifier are shown in Fig. 3. As can be seen, equal magnitude and 180° phase delay have been achieved at the gate and drain, which confirms the push-pull operation of this circuit.

To examine the performance of the push-pull power amplifier, a single device class B power amplifier with quarter-wave-

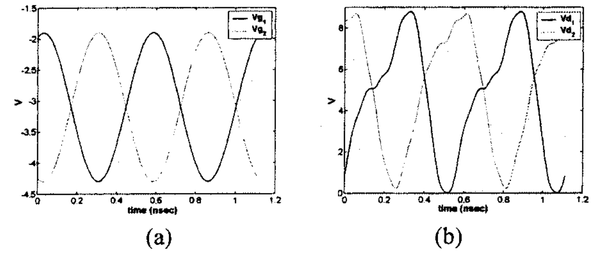

Fig. 3. Simulated gate voltage (a) and drain voltage (b) for each device in the push-pull power amplifier.

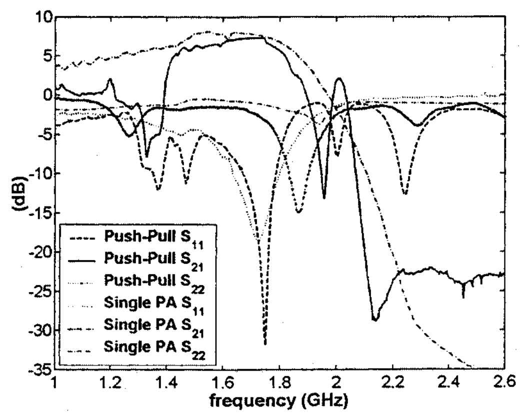

Fig. 4. Measured large-signal gain and return loss for the push-pull PA and single class B PA.

length stubs as even harmonic terminations is also fabricated on the same substrate as a reference. Both circuits are operated at the class B bias point, with $Vds = 5.0$ V and $Vgs = -3.1$ V. The measured small-signal gain and return loss of the single class B power amplifier and the extended resonance push-pull amplifier are shown in Fig. 4. The gain of the single class B amplifier at 1.75 GHz is 7.9 dB with return loss of -16.5 dB while the push-pull class B amplifier provides a gain of 7.3 dB with return loss of -31.9 dB. The 1-dB bandwidth for the single class B amplifier and push-pull PA are 0.33 GHz and 0.22 GHz, respectively.

The output power and the PAE of the single class B and push-pull power amplifier are measured as a function of input power at 1.75 GHz (Fig. 5). The measured output power of the single class B amplifier under 1-dB gain compression is 27.3 dBm with PAE of 61%, and the measured output power of the push-pull power amplifier design under 1-dB compression is 30 dBm with PAE of 59%. Based on the above values, the class B push-pull design achieves a power combining efficiency (PCE) of 93%.

A two-tone measurement to determine the third order intermodulation distortion of the class B push-pull power amplifier was also performed. The measured IP3 point is approximately 42 dBm, 12 dB above the $P_{\rm 1dB}$ point and the measured IP3 point for the single class B power amplifier is 36 dBm, which is 8.7 dB above the single class B power amplifier's $P_{\rm 1dB}$ point. By biasing the circuit into class AB operation, the IP3 point of the push-pull power amplifier can be improved. In our design, when the Vgs at gates was increased from -3.1 V to -2.7 V, the measured $IP3_{\rm out}$ increased by 8 dB to 50 dBm without any noticeable change in output power and PAE.

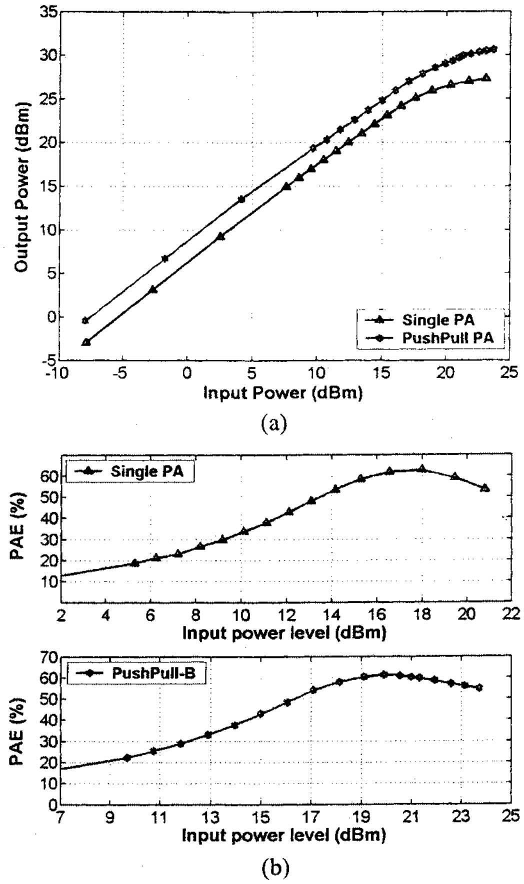

Fig. 5. Output power (a) and PAE (b) for the push-pull and single class B power amplifier at 1.75 GHz.

IV. Conclusion

In this paper, a class B push-pull power amplifier is designed based on the extended resonance power dividing/combining technique. At the center frequency of 1.75 GHz, the output power at 1-dB compression is 30 dBm with the PAE of 59% and a power combining efficiency of 93%. The measured IP3 point is 12 dB above the P_{1dB} point. Based on this push-pull extended resonance technique, we are now designing the integrated circuit power amplifiers at RF/microwave frequencies.

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